IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

	ATTY. DOCKET NO.:	**BUR920000198US1**
IN RE APPLICATION OF:	§	
	§	
JON DAVID GARLETT	§ EXAMINER:	**YOUNG TOI TSE**
	§	
SERIAL NO.: **10/064,387**	§ CONFIRMATION NO.:	**5830**
	§	
FILED: **JULY 9, 2002**	§ ART UNIT:	**2611**
	§	
FOR: **DATA COMMUNICATION SYSTEM WITH SELF-TEST FEATURE**	§	
	§	
	§	

AMENDMENT D UNDER 37 C.F.R. § 1.116

MAIL STOP AMENDMENT
COMMISSIONER FOR PATENTS
PO BOX 1450
ALEXANDRIA, VIRGINIA 22313-1450

SIR:

This Amendment is submitted in response to the Examiner's Advisory Action dated July 27, 2007. The Advisory Action was issued pursuant to an Amendment in response to the Final Action dated May 17, 2007, having a shortened statutory period set to expire August 17, 2007. No fee is believed to be required to submit this amendment. However, in the event any fees are necessary to further the prosecution of this application, please charge the fees to **IBM CORPORATION'S Deposit Account No. 09-0456**.

AMENDMENTS IN THE CLAIMS

1-16. (canceled)

17. (currently amended) A data communication system comprising:

a random digital sequence generator (~~"sequence generator"~~) capable of selectively issuing a series of digital 1 and 0 bits in a random sequence; and

an activate circuit coupled to an output of the sequence generator and which responds to receipt of a pre-set sequence of digital bits from the sequence generator by initiating a self-test operation by which the data communication system dynamically adjusts, on a random basis, a time period in which data windows are present within transmitting data signals, wherein the pre-set sequence indicates transmission of test data and addition of jitter to the system to perform the self-test operation.

18. (currently amended) The data communication system of Claim 17, further comprising means for introducing jitter within the data communication system and activating a self test mechanism by generating [[a]] the pre-set sequence of digital bits from the random digital sequence generator as the test data.

19. (currently amended) The data communication system of Claim 17, wherein the activate circuit comprises a time adjust system that adjusts [[the]] a time period of the data windows by delaying an opening, leading edge of the data window.

20. (currently amended) The data communication system of Claim 17, wherein the activate circuit comprises a time adjust system that adjusts [[the]] a time period of the data windows by advancing a closing, trailing edge of the data window.

21. (currently amended) The data communication system of Claim 17, wherein the activate circuit comprises:

a plurality of latches which receive even and odd alternating bits of an original sequence of incoming data bits;